detection mechanism is strongly dependent on diode bias and in order to use the diode in a regenerative mode the diode will have to be biased stably in the negative resistance region. The application of the diode in doppler systems is also limited because of the noise associated with the device. The origin or characteristics of this noise are not understood presently but may be related to low frequency bias circuit oscillations.

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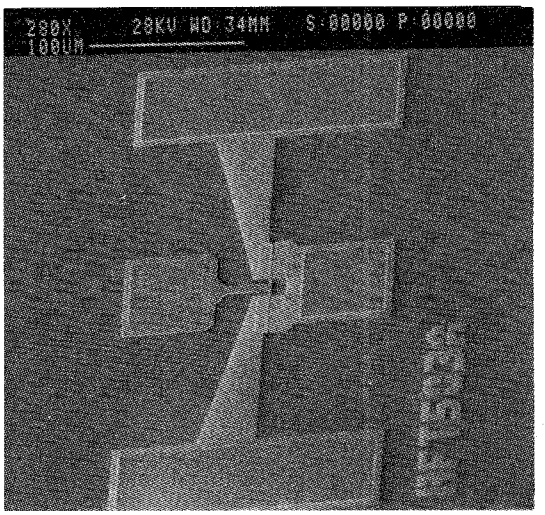

Fig. 1. A typical 0.25 × 50 micron cascade probed MESFET.

TABLE I
AVERAGE VALUE AND STANDARD DEVIATION OF f_t AND C_{total} AT $V_{ds} = 3$ V

Gate Width	Gm (mS/mm)		ft (GHz)		C_{total}(pf)	
	Ave.	S.D.	Ave.	S.D.	Ave.	S.D.
50 μ	458	21	82.9	1.9	0.044	0.001
100 μ	440	14	97.2	4.2	0.072	0.002
150 μ	437	14	104.2	4.6	0.100	0.003
200 μ	428	16	107.8	1.8	0.126	0.003

A Technique for Correction of Parasitic Capacitance on Microwave f_t Measurements of MESFET and HEMT Devices

Milton Feng, C. L. Lau, and C. Ito

Abstract—**The current gain cutoff frequency, f_t, has become a critical figure-of-merit for evaluating performance of MESFET and HEMT devices. The f_t is related to a capacitance parameter, C_{tot}, through the equation $f_t = Gm/(2\pi C_{tot})$. This capacitance, however, includes a parasitic component primarily due to contact pad and device geometry as well as a parasitic component due to Rd, Rs and Rds. This paper describes a technique which determines this parasitic capacitance for FET-type devices. Consistently accurate corrections can then be made to reported f_t values. Ion implanted InGaAs MESFET's with 0.25 μ gate lengths have achieved 120 GHz f_t before correction and 151 GHz f_t after correction.**

I. INTRODUCTION

The accuracy of microwave f_t measurements has become an important issue since this parameter is widely used as a figure-of-merit for speed and frequency evaluation of MESFET and HEMT devices. Currently, microwave devices are characterized on-wafer from 45 MHz to 26.5 GHz using Cascade RF probes and Cascade calibration standards on quartz substrates. The current gain, $|H_{21}|$, of the device is calculated from measured S-parameters and f_t is determined by extrapolating $|H_{21}|$ using a slope of -6 dB/octave down to the unity current gain point. Fundamentally after calibration, f_t should be independent of device gate width and only scale with gate length.

However, in a recent work [1], the $|H_{21}|$ vs. frequency plot shows a dependence on gate width. In addition, the ratio of f_t for 0.1 micron gate device to that of a 0.2 μ gate device should approach 2 rather than 1.1 as the work indicates. These discrepancies can be attributed to inaccurate calibration and parasitic capacitance corrections.

In this work, we show that the f_t dependence on gate width is mainly due to the parasitic capacitance associated with the pad layout of the device. An accurate technique is then presented for determination of the parasitic capacitance of MESFET and HEMT devices.

II. EXPERIMENTAL CASCADE f_t DATA

The ion implanted InGaAs MESFET's used in this work have 0.25 μ long "T" shaped gates with total gate widths of 200, 150, 100, and 50 μ. The device pad layout is the same for all gate width variations and a typical device (50 μ gate width) is shown in Fig. 1. Over 15 devices of each gate width are used to determine the average f_t value at $V_{ds} = 3.0$ V and its standard deviation as listed in Table I.

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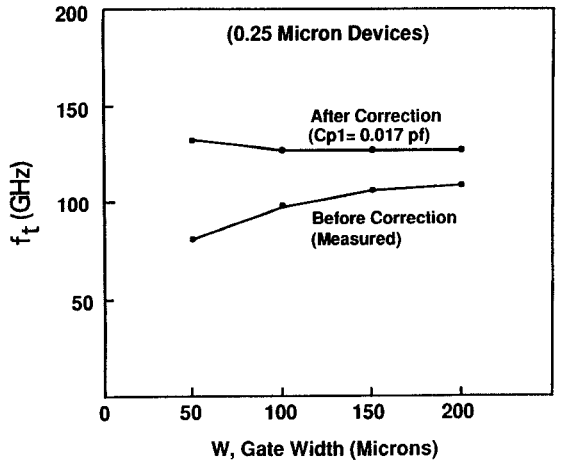

Fig. 2. f_t versus gate width before/after parasitic capacitance correction of $Cp2/Cw$.

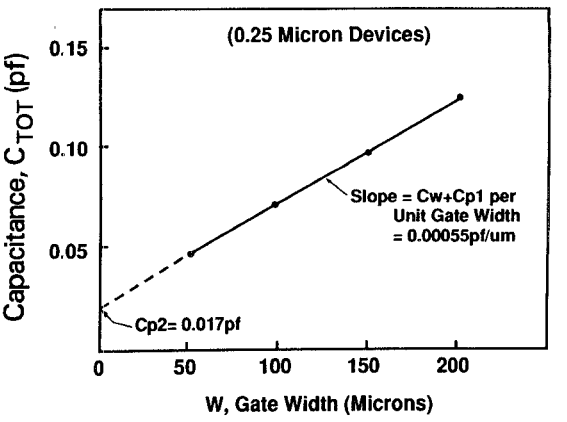

Fig. 3. Total capacitance versus gate width.

TABLE II
AN EQUIVALENT CIRCUIT MODEL FOR AN 0.25×200 μ GATE MESFET AT Vds = 3 V

Elements	100% Idss	50% Idss	20% Idss
Re (Ω)	0.58	0.56	0.39
Rd (Ω)	2.39	2.03	1.13
Rds (Ω)	115	108	123
gm (mS)	85	68	43
Cgs (pf)	0.097	0.079	0.065
Cgd (pf)	0.012	0.015	0.018

The Cascade probes are calibrated using the Impedance Standard Quartz Substrate (ISS) supplied by Cascade Microtech. The measured f_t before correction for parasitic capacitance is therefore dependent on gate width as shown in Fig. 2. The f_t for the 50 μ gate width device is lower than for the 200 μ device by about 23%.

III. Current Gain Cutoff Frequency Equation

The intrinsic f_t equation for the short-circuit current gain of a FET or HEMT is expressed as

$$f_t = \frac{\mathrm{Gm}}{2\pi(\mathrm{Cgs}+\mathrm{Cgd})} \tag{1}$$

where Gm is the transconductance, Cgs is the gate-to-source capacitance, and Cgd is the gate-to-drain capacitance. Tasker, *et al.* [2] reported a more rigorous derivation for the extrinsic f_t which takes source and drain resistance into account:

$$f_t = \frac{\mathrm{Gm}}{2\pi\{(\mathrm{Cgs}+\mathrm{Cgd})[1+(\mathrm{Rs}+\mathrm{Rd})/\mathrm{Rds}]+\mathrm{Cgd}^*\mathrm{Gm}^*(\mathrm{Rs}+\mathrm{Rd})\}} \tag{2}$$

where Rs is the source resistance, Rd is the drain resistance and Rds is the drain to source resistance. The equivalent circuit elements Gm, Cgs, and Cgd are directly proportional and Rs, Rd, and Rds are inversely proportional to gate width. Hence, in either equation the gate width dependence cancels out leaving f_t independent of gate width. Hence, any measured f_t values which exhibit gate width dependence are not in agreement with the above equations because of parasitic capacitance effects.

IV. Parasitic Capacitance

The capacitance term in the denominator of (2) for f_t, which includes a parasitic capacitance, can be represented as the sum of two components: C_w and C_{p1}. The first term, C_w, = Cgs + Cgd, is dependent on gate width, w, and is equal to the intrinsic capacitance in the denominator of equation (1). The second term, $C_{p1} = (\mathrm{Cgs}+\mathrm{Cgd})[(\mathrm{Rs}+\mathrm{Rd})/\mathrm{Rds}]+\mathrm{Cgd}^*\mathrm{Gm}^*(\mathrm{Rs}+\mathrm{Rd})$, is the parasitic capacitance which scales with gate width. The Cp1 term is due to Rd and Rs in the FET's. The presence of Rd and Rs requires current flow through Rds in order to compensate for voltage drop in Cgs and Cgd. In addition, the parasitic capacitance associated with pad and device geometry is, however, not included in (2). Hence, a third term, C_{p2}, is required in (2) for a constant parasitic capacitance which is independent of gate width. The total parasitic capacitance of the device is the sum of $C_{p1}+C_{p2}$. Therefore, the measured value of f_t can be written as

$$f_t = \frac{\mathrm{Gm}}{2\pi(C_w + C_{p1} + C_{p2})} \tag{3}$$

Rearranging (3), the total capacitance is equal to

$$C_{\mathrm{tot}} = C_w(w) + C_{p1}(w) + C_{p2} = \frac{\mathrm{Gm}}{2\pi f_t} \tag{4}$$

Equation (4) can be plotted versus gate width for a series of MESFET's with varying gate widths, but with the same pad layout. The intercept corresponding to zero gate width is equal to C_{p2}, the constant parasitic capacitance.

V. Experimental Verification

The measured data for the 0.25 μ gate length MESFET's used in this work is listed in Table I. When C_{tot} was calculated, the microwave transconductance (Gm) was extracted from S_{21} at 2 GHz.

C_{tot} versus gate width (biased at 100% Idss) is plotted in Fig. 3. The C_{tot} values for 50, 100, 150, and 200 μ devices are colinear; the intercept at zero gate width is equal to C_{p2} and has a value of 0.0169 pf using a least squares fit. The term $C_w + C_{p1} = C_{\mathrm{tot}} - C_{p2}$ is then used to calculate a new f_t value which is corrected for the constant portion of the parasitic capacitance and is shown in Fig. 2.

Since C_{p1} is dependent on the gate width and drain bias as pointed out in reference [2], at large drain bias voltages, (1) is adequate for measuring f_t. However, at low drain bias voltages (less than or equal of knee voltage), (2) is required to measure f_t. An equivalent circuit model for a typical 0.25×200 micron gate MESFET is characterized by S-parameters measured from 1 to 25 GHz at $V_{ds} = 3$ V. The elements Rd, Rs, Rds, Gm, Cgs, and Cgd to estimate the Cp1 of this MESFET model are listed

TABLE III
ESTIMATION OF $Cp1/Cw$ AT Vds = 3 V

Expression	100% Idss	50% Idss	20% Idss
(Rs+Rd)/Rds	0.0258	0.0247	0.012
Cgd*Gm*(Rs+Rd)/(Cgd+Cgs)	0.0278	0.0281	0.0142
$Cp1/Cw$	0.0536	0.0528	0.0252

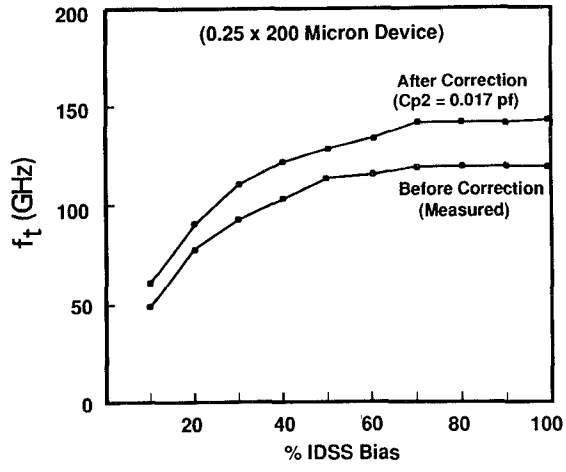

Fig. 4. f_t versus % Idss before/after parasitic capacitance correction of $Cp2/Cw$ as a function of gate biases.

in Table II at 100% Idss, 50% Idss, and 20% Idss. The (Rs+Rd)/Rds term and the Cgd*Gm*(Rd+Rs)/(Cgd+Cgs) term are calculated and listed in Table III to indicate percentage error to (Cgs+Cgd). The $Cp1/Cw = 5.4\%$ at 100% Idss and 2.5% at 20% Idss and agree well with HEMT result at high Vds as reported in [2]. $Cp2/Cw = 16\%$ and $Cp1/Cw = 5\%$ is the correction for the 0.25×200 μ gate FET and the $Cp2/Cw = 63\%$ and $Cp1/Cw = 5\%$ is the correction for the 0.25×50 μ gate FET. Consequently, $Cp2/Cw$ can be a very large correction term as gate width decreases to below 50 μ.

Next, the f_t dependence on gate bias for a 0.25×200 μ, ion implanted InGaAs MESFET is measured. We applied the above parasitic capacitance correction technique and compared the f_t before and after correction as shown in Fig. 4. Before the correction, the peak f_t is 120 GHz and the f_t values are greater than 100 GHz for biases from 40% to 100% Idss. After correction of $Cp2/Cw = 16\%$, the peak value of f_t is 143 GHz and the f_t values are greater than 100 GHz for bias ranges from 25% to 100% Idss as shown in Fig. 4. At low gate bias, the f_t correction is small because the transconductance is low. Finally, after correction of both $Cp2/Cw = 16\%$ and $Cp1/Cw = 5\%$, the peak f_t is 151 GHz for the measured f_t value of 120 GHz indicating excellent millimeter-wave performance comparable to pseudomorphic HEMT's.

VI. Conclusion

We have described a technique for determining the parasitic capacitance attributed to device layout geometry. This simple technique for determining the parasitic capacitance attributed to device layout geometry. This simple technique requires only on-wafer, Cascade probe measurements on devices with varying gate widths. This technique will assist in the optimization of device layout design and in improving device modeling performance for microwave and millimeter-wave applications.

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Accurate Measurement of Signals Close to the Noise Floor on a Spectrum Analyzer

Andrew A. Moulthrop and Michael S. Muha

Abstract—**Because most spectrum analyzers are calibrated to read the true power of a sinusoidal signal, a correction factor is necessary to read the true power of a nonsinusoidal signal, such as noise. Consequently, when noise and a sine wave are both present, a correction factor that is a function of the signal-to-noise ratio is necessary to find the true signal power. For some spectrum analyzers the correction factor for pure noise is incorporated into the software, but the correction factor for signal plus noise is generally ignored. This article derives this correction factor, which is significant where the signal-to-noise ratio is near unity.**

Introduction

Spectrum analyzers are commonly used to measure sinusoidal signals close to the noise floor of the measurement system. For example, measuring the third-order intercept of a small-signal amplifier requires an accurate determination of the amplitude of the third-order intermodulation products, which are usually close to the noise floor. In this case, the spectrum analyzer's internally generated distortion products, in addition to noise, can reduce the accuracy of the amplitude measurement. Since the internally generated distortion products have an unknown phase with respect to the desired signal, it is not generally possible to correct for these products; rather, one must avoid them entirely, by attenuating the input signal. Attenuating this input signal will decrease the signal-to-noise ratio, unless a feedforward cancellation technique [1] is used. In any case, noise remains as a limitation of measurement accuracy. It is possible, however, to correct for noise in the amplitude measurement, because noise causes a deterministic error. This error is deterministic because, although the noise amplitude fluctuates randomly, these fluctuations can be smoothed by using a narrow video filter or by video averaging. The signal peak can then be measured accurately; however, this power measurement includes both signal power and noise power.

One might try (naively) to correct for noise by subtracting the displayed noise power from the power of the displayed signal plus noise, but such a correction can result in a larger error than if the noise is simply ignored. This is because spectrum analyzers

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